REMARKS

In the Office Action of October 20, 2004, the Examiner allowed claims 1-8, objected to claims 11 and 14 as being dependent on a rejected base claim, and rejected claims 9, 10, 12, 13, and 15-19. More particularly, regarding the claim rejections, the Examiner rejected claims 9, 10, 15, and 17-19 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,768,738 to Yazaki et al. ("Yazaki"); rejected claims 12 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Yazaki in view of U.S. Patent No. 6,577,636 to Sang et al. ("Sang"); and rejected claim 16 under 35 U.S.C. § 103(a) as being unpatentable over Yazaki in view of U.S. Patent No. 6,763,023 to Gleeson et al. ("Gleeson").

By this Amendment, Applicants have amended the specification to include the serial number and filing date of the application referenced in the "Related Applications" section of the application.

For the following reasons, Applicants respectfully traverse the rejection of claims 9, 10, 15, and 17-19 based on Yazaki.

Claim 9 is directed to a multiport device including a plurality of receive ports, a plurality of transmit ports, an internal rules checking circuit, and a port vector queue. The receive ports receive frames in a packet-switched network, the frames having a source field indicating the source of the frame and a destination field indicating an intended destination for the frame. The transmit ports are configured to transmit the frames in the packet-switched network. The internal rules checking circuit is coupled to receive input frame header information from the receive ports and configured to determine frame forwarding information that indicates which of the plurality of transmit ports the received frames should be transmitted from. The internal rules checking circuit includes a plurality of frame lookup components operating in parallel, each of the plurality of frame lookup components being associated with an address table, synchronously receive the frame header information

received by the internal rules checking circuit, and identify the frame forwarding information for the received frame header information from the address table associated with the frame lookup component. The port vector queue is connected to the internal rules checking circuit, the port vector queue receiving the frame forwarding information identified by the internal rules checking circuit and forwarding the frame forwarding information to appropriate ones of the transmit ports.

Yazaki does not disclose each of the elements recited in claim 9. Yazaki, for example, does not disclose the internal rules checking circuit recited in claim 9. In particular, the internal rules checking circuit of claim 9 includes "a plurality of frame lookup components operating in parallel, each of the plurality of frame lookup components being associated with an address table, synchronously receiving the frame header information received by the internal rules checking circuit, and identifying the frame forwarding information for the received frame header information from the address table associated with the frame lookup component." Yazaki completely fails to disclose this aspect of the invention recited in claim 9.

Yazaki is directed to a packet forwarding apparatus. (Yazaki, Title). The packet forwarding apparatus includes a routing processing unit, a flow detection unit, and a packet forwarding unit. (Yazaki, Abstract). The flow detection unit, in particular, is shown by Yazaki as flow detector 112 (Fig. 1), and is generally described in column 13:

> On the other hand, the flow detector 112 detects or retrieves an entry table 750 (or 551) based on the header information 11 received from the output FIFO allocation circuit 121 to determine priority information on the received packet and outputs the priority information to the output FIFO allocation circuit 121 as packet priority information 13. When the output FIFO allocation circuit 121 receives the packet priority information 13 therein, it writes it into the header of the corresponding packet stored in the buffer memory 128 as QoS control information 409.

(Yazaki, column 13, lines 56-64). As described in this section of Yazaki, flow detector 112 appears to generally relate to determining priority information of the received packets.

In rejecting claim 9, the Examiner contends that the recited internal rules checking circuit corresponds to unit 110 (Fig. 1) of Yazaki. More specifically, regarding "the plurality of frame lookup components operating in parallel" recited in claim 9, the Examiner points to Fig. 12 and elements 730 and 740 of Yazaki. Fig. 12 of Yazaki is a diagram of flow detector 112. As discussed above, flow detector 112 determines priority information of received packets. Flow detector 112, and thus elements 730 and 740, does not correspond to the frame lookup components recited in claim 9, which are part of the internal rules checking circuit that determines "frame forwarding information that indicates which of the plurality of transmit ports the received frames should be transmitted from." A flow detector that determines priority information is not equivalent to the internal rules checking circuit recited in claim 1.

As further evidence that tables 730 and 740 of Yazaki could not correspond to the plurality of frame lookup components recited in claim 9, Applicants note that elements 730 and 740 are used for different functions by Yazaki. Element 730 is a "list table read out unit 730" and is described at column 14, line 57 through column 15, line 13. Element 740 is an "entry table read out unit 740" and is described at column 15, lines 13-30. Accordingly, Applicants submit that it is not appropriate to contend that units 730 and 740 could correspond to the plurality of frame lookup components recited in claim 9.

Moreover, Applicants note that each of the plurality of frame lookup components of claim 9 are specifically recited as "being associated with an address table, synchronously receiving the frame header information received by the internal rules checking circuit, and identifying the frame forwarding information for the received frame header information from the address table associated with the frame lookup component." Neither unit 730 nor unit 740 of Yazaki can be said to correspond to such a frame lookup component. The Examiner points to Fig. 12 and column 14, lines 46-56 of Yazaki as allegedly disclosing these features. This section of Yazaki states:

> When header information 11 of a packet is transmitted from the packet I/O unit 120 to the header processing unit 110, the start of detection 600 is executed and the flow detector 112 stores input line numbers 407, SIP 402, DIP 403, SPORT 404, DPORT 405 and TOS 411 included in the header information 11 into an I/O line number storage 732 provided within the list table read out unit 730, and a packet SIP storage 722-2, a packet DIP storage 723-2, a packet SPORT storage 724-2, a packet DPORT storage 725-2 and a packet TOS storage 728-2 provided within the condition check unit 720 respectively (Step 601).

(Yazaki, column 14, lines 46-56). Although this section Yazaki generally discloses reading information from a table, it in no way discloses or suggests the frame lookup components recited in claim 9.

For at least these reasons, Applicants submit that Yazaki does not disclose or suggest each element recited in claim 9. Accordingly, the rejection of claim 9 under 35 U.S.C. § 102(e) is improper and should be withdrawn. The rejections of claims 10 and 15 based on Yazaki should also be withdrawn, at least by virtue of their dependency from claim 10.

Claims 17-19 were additionally rejected by the Examiner under 35 U.S.C. § 102(e) in view of Yazaki. Claim 17 is directed to a method of determining frame forwarding information for frames received in a network device. The method includes, among other things, distributing the frames among a plurality of frame lookup components implemented in parallel with one another, each of the frame lookup components coupled to an associated address table and configured to look up a frame forwarding descriptor for each of the received frames from the associated address table, the frame forwarding descriptor identifying the frame forwarding information. As mentioned above, Yazaki does not disclose "a plurality of frame lookup components implemented in parallel with one another," as is recited in claim 17. Units 730 and 740, which are pointed to by the Examiner as corresponding to the claimed plurality of frame lookup components, each implement different functions. Further, as is mentioned above, neither of units 730 or 740 is coupled to an associated address table and configured to look up a frame forwarding descriptor for each of the

received frames from the associated address table, the frame forwarding descriptor identifying the frame forwarding information, as is recited in claim 17.

For at least these reasons, Applicants submit that Yazaki does not disclose or suggest each element recited in claim 17. Accordingly, the rejection of claim 17 under 35 U.S.C. § 102(e) is improper and should be withdrawn. The rejection of claim 18 based on Yazaki should also be withdrawn, at least by virtue of its dependency from claim 17.

Independent claim 19 is directed to a multiport device including, among other things, means for distributing frames among a plurality of frame lookup components implemented in parallel with one another, each of the frame lookup components coupled to an associated address table and configured to identify a frame forwarding descriptor for each of the received frames from the address table, the frame forwarding descriptor identifying the frame forwarding information. For reasons similar to those previously discussed with respect to claims 9 and 17, Applicants submit that Yazaki does not disclose each of the features of claim 19. Accordingly, the rejection of this claim should also be withdrawn.

Claims 12 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yazaki in view of Sang. Applicants submit that this rejection is not a proper rejection under 35 U.S.C. § 103(a), as Sang does not qualify as prior art under 35 U.S.C. § 103(a). 35 U.S.C. § 103(c) qualifies 35 U.S.C. § 103(a) and states:

> (c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

(35 U.S.C. § 103(c)). Sang qualifies as prior art under 35 U.S.C. § 102 only under subsection (e), and Sang and the pending application are both assigned to Advanced Micro Devices, Inc.

Accordingly, Sang is not available to preclude patentability under 35 U.S.C. § 103(a). For at least these reasons, the rejection of claims 12 and 13 is improper and should be withdrawn.

Claim 16 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yazaki in view of Gleeson. Claim 16 depends from claim 10. Although Applicants do not necessarily agree with the Examiner's interpretation of Gleeson, Applicants submit that Gleeson does not cure the above-discussed deficiencies of Yazaki with regard to claim 10. Accordingly, the rejection of claim 16 based on Yazaki and Gleeson should be withdrawn.

In view of the foregoing amendments and remarks, Applicants respectfully request withdrawal of the outstanding rejections and the timely allowance of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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